Amendment To The Claims

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a first conductive type semiconductor layer;

at least one first unit cell including a first conductive type first semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the first semiconductor region to a line; ~~and~~

at least one second unit cell including a second conductive type second semiconductor region formed in the first conductive type semiconductor layer and a contact region for electrically connecting the second semiconductor region to a line[[,]]; and

element isolation region located between the first unit cell and the second unit cell;

wherein the first unit cell and the second unit cell act as a diode element in cooperation.

2. (Original) The semiconductor device according to claim 1, wherein the at least one first unit cell is a plurality of first unit cells and the at least one second unit cell is a plurality of second unit cells.

3. (Previously presented) The semiconductor device according to claim 1, wherein a dimension that defines a size of each of the first semiconductor region and the second semiconductor region is substantially a same as a minimum dimension that is allowed by a design rule for the semiconductor device.

4. (Previously presented) The semiconductor device according to claim 1, wherein

each of the first semiconductor region and the second semiconductor region viewed from a normal line direction is substantially square in shape.

5. (Previously presented) The semiconductor device according to claim 1, wherein the first unit cells and the second unit cells are arranged in a checkered pattern in the first conductive type semiconductor layer.

6. (Previously presented) The semiconductor device according to claim 1, wherein the first unit cell and the second unit cell are arranged in the first conductive type semiconductor layer with a predetermined distance to each other, and on an intercell region that is positioned between the first unit cell and the second unit cell in the first conductive type semiconductor layer, a gate electrode structure including at least an insulating layer formed on the cell region and a conductive layer formed on the insulating layer is formed.

7. (Original) The semiconductor device according to claim 6, further comprising a gate line electrically connected to the gate electrode structure.

8. (Original) The semiconductor device according to claim 1, wherein a plurality of second unit cells are formed in the first semiconductor region of one first unit cell.

9. (Previously presented) The semiconductor device according to claim 1, further comprising a second conductive type semiconductor layer, wherein the first conductive type semiconductor layer is formed on the second conductive type semiconductor layer.

10. (Original) The semiconductor device according to claim 9, wherein the first unit cell formed in the first conductive type semiconductor layer is used as a base, and the second unit cell is used as an emitter, and the second conductive type semiconductor layer is used as a collector.

11. (Previously presented) The semiconductor device according to claim 9, wherein the second conductive type semiconductor layer is a semiconductor substrate, and the first conductive type semiconductor layer is a well region formed in the semiconductor substrate.

12. (Previously presented) The semiconductor device according to claim 1, wherein the first conductive type semiconductor layer is formed on an insulating layer.

13. (Previously presented) The semiconductor device according to claim 1, further comprising an analog circuit section and a digital circuit section, wherein the diode element is formed in the analog circuit section, and the analog circuit section and the digital circuit section are produced by a CMOS process.